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WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a doped buried layer located over a doped substrate;

a doped epitaxial layer located over the doped buried layer;

a first doped lattice matching layer located between the doped substrate and the doped buried layer; and

a second doped lattice matching layer located between the doped buried layer and the doped epitaxial layer.

2. The semiconductor device as recited in Claim 1 wherein dopant concentrations of the first and second doped lattice matching layers are each less than a dopant concentration of the doped buried layer.

3. The semiconductor device as recited in Claim 2 wherein a dopant concentration of the doped substrate is less than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the doped epitaxial layer is less than the dopant concentration of the second doped lattice matching layer.

4. The semiconductor device as recited in Claim 2 further including a third doped lattice matching layer located between the

first doped lattice matching layer and the doped buried layer and a fourth doped lattice matching layer located between the second doped lattice matching layer and the doped buried layer.

5. The semiconductor device as recited in Claim 4 wherein a dopant concentration of the third doped lattice matching layer is more than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the fourth doped lattice matching layer is more than the dopant concentration of the second doped lattice matching layer.

6. The semiconductor device as recited in Claim 3 wherein the dopant concentration of the doped substrate ranges from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3, the dopant concentrations of the doped buried layer ranges from about 1E19 atoms/cm^3 to about 1E20 atoms/cm^3, and the dopant concentration of each of the first and second doped lattice matching layers ranges from about 1E15 atoms/cm^3 to about 1E19 atoms/cm^3.

7. The semiconductor device as recited in Claim 1 wherein the first and second doped lattice matching layers each include a dopant gradient wherein a dopant concentration of each of the dopant gradients is greater adjacent the doped buried layer.

8. A method of manufacturing a semiconductor device, comprising:

forming a first doped lattice matching layer over a doped substrate;

creating a doped buried layer over the first doped lattice matching layer;

producing a second doped lattice matching layer over the doped buried layer; and

placing a doped epitaxial layer over the second doped lattice matching layer.

9. The method as recited in Claim 8 wherein forming and producing includes forming and producing first and second doped lattice matching layers each having a dopant concentration less than a dopant concentration of the doped buried layer.

10. The method as recited in Claim 9 wherein a dopant concentration of the doped substrate is less than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the doped epitaxial layer is less than the dopant concentration of the second doped lattice matching layer.

11. The method as recited in Claim 9 further including

forming a third doped lattice matching layer between the first doped lattice matching layer and the doped buried layer and forming a fourth doped lattice matching layer between the second doped lattice matching layer and the doped buried layer.

12. The method as recited in Claim 11 wherein a dopant concentration of the third doped lattice matching layer is greater than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the fourth doped lattice matching layer is greater than the dopant concentration of the fourth doped lattice matching layer.

13. The method as recited in Claim 10 wherein the dopant concentration of the doped substrate ranges from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3, the dopant concentration of the doped buried layer ranges from about 1E19 atoms/cm^3 to about 1E20 atoms/cm^3, and each of the dopant concentrations of the first and second doped lattice matching layers range from about 1E15 atoms/cm^3 to about 1E19 atoms/cm^3.

14. The method as recited in Claim 8 wherein forming and producing each of the first and second doped lattice matching layers includes forming and producing a dopant gradient wherein a

dopant concentration of each of the dopant gradients is greater adjacent the doped buried layer.

15. The method as recited in Claim 8 wherein forming, creating, producing, and placing, includes forming, creating, producing, and placing using a chemical vapor deposition process.

16. The method as recited in Claim 15 wherein forming, creating, producing, and placing using a chemical vapor deposition process includes forming, creating, producing, and placing in a single deposition chamber.

17. A integrated circuit, comprising:

a doped buried layer located over a doped substrate;

a doped epitaxial layer located over the doped buried layer;

a first doped lattice matching layer located between the doped substrate and the doped buried layer; and

a second doped lattice matching layer located between the doped buried layer and the doped epitaxial layer;

transistors located over the doped epitaxial layer; and

interconnects located within interlevel dielectric layers located over the transistors, which connect the transistors to form an operational integrated circuit.

18. The integrated circuit as recited in Claim 17 wherein dopant concentrations of the first and second doped lattice matching layers are each less than a dopant concentration of the doped buried layer.

19. The integrated circuit as recited in Claim 18 wherein a dopant concentration of the doped substrate is less than the dopant concentration of the first doped lattice matching layer and a dopant concentration of the doped epitaxial layer is less than the dopant concentration of the second doped lattice matching layer.

20. The integrated circuit as recited in Claim 17 further including additional active and passive devices.

21. A semiconductor device, comprising:

a co-doped germanium buried layer located over a doped substrate;

a doped epitaxial layer located over the co-doped germanium buried layer.

22. The semiconductor device as recited in Claim 21 wherein the co-doped germanium buried layer includes a p-type dopant.

23. The semiconductor device as recited in Claim 22 wherein the p-type dopant is boron.

24. The semiconductor device as recited in Claim 21 wherein a dopant concentration of the co-doped germanium buried layer ranges from about 1E15 atoms/cm^3 to about 1E20 atoms/cm^3, a dopant concentration of the doped substrate ranges from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3, and a dopant concentration of the doped epitaxial layer ranges from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3.

25. The semiconductor device as recited in Claim 21 wherein the co-doped germanium buried layer has a germanium concentration ranging from about 2E20 atoms/cm^3 to about 7E20 atoms/cm^3.

26. The semiconductor device as recited in Claim 21 wherein the co-doped germanium buried layer has a thickness ranging from about 1 μm to about 10 μm.

27. The semiconductor device as recited in Claim 21 wherein the doped substrate, co-doped germanium buried layer, and the doped epitaxial layer collectively have a thickness ranging from about 2 μm to about 20 μm.

28. A method of manufacturing a semiconductor device, comprising:

forming a co-doped germanium buried layer over a doped substrate;

creating a doped epitaxial layer over the co-doped germanium buried layer.

29. The method as recited in Claim 28 wherein forming the co-doped germanium buried layer includes forming the co-doped germanium layer with a p-type dopant.

30. The method as recited in Claim 29 wherein the p-type dopant is boron.

31. The method as recited in Claim 28 wherein forming includes forming the co-doped germanium buried layer having a dopant concentration ranging from about 1E15 atoms/cm^3 to about 1E20 atoms/cm^3 over the doped substrate having a dopant concentration ranging from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3, and creating includes creating the doped epitaxial layer having a dopant concentration ranging from about 1E14 atoms/cm^3 to about 1E15 atoms/cm^3.

32. The method as recited in Claim 28 wherein forming includes forming the co-doped germanium buried layer having a germanium concentration ranging from about 2E20 atoms/cm^3 to about 7E20 atoms/cm^3.

33. The method as recited in Claim 28 wherein forming includes forming the co-doped germanium buried layer having a thickness ranging from about 1 μm to about 10 μm.

34. The method as recited in Claim 28 wherein the doped substrate, co-doped germanium buried layer, and the doped epitaxial layer collectively have a thickness ranging from about 2 μm to about 20 μm.

35. The method as recited in Claim 28 wherein forming and creating includes forming and creating using a chemical vapor deposition process.

36. The method as recited in Claim 35 wherein forming and creating includes forming an creating in a single deposition chamber.

37. An integrated circuit, comprising:

a co-doped germanium buried layer located over a doped substrate;

a doped epitaxial layer located over the co-doped germanium buried layer;

transistors located over the doped epitaxial layer; and

interconnects located within interlevel dielectric layers located over the transistors, which connect the transistors to form an operational integrated circuit.

38. The integrated circuit as recited in Claim 37 wherein the co-doped germanium buried layer further includes boron.

39. The integrated circuit as recited in Claim 37 wherein the co-doped germanium buried layer has a germanium concentration ranging from about 2E20 atoms/cm^3 to about 7E20 atoms/cm^3.

40. The integrated circuit as recited in Claim 37 further including additional active and passive devices.